2841

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	OLIVIER BOIREAU		
For:	INTEGRATED CIRCUIT PACKAGE AND PRINTED CIRCUIT BOARD ARRANGEMENT		
Serial No.:	10/065,016	Examiner:	
Filed:	September 10, 2002	Group Art Unit:	2841
Docket No.:	71522-2		

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Sir:

TRANSMITTAL OF PRIORITY DOCUMENT

Applicant submits herewith a certified copy of the priority document (United Kingdom Application No. 0121891.6) relied upon by Applicant in the captioned application, pursuant to 37 C.F.R. § 1.55(a)(2).

Please direct any questions relating to this matter to the undersigned attorney for Applicant.

Respectfully submitted,

Olivier Boireau

Date: 10 January 2003

By: _____

Joel E. Bair, Reg. No. 33,356
McGARRY BAIR PC
171 Monroe Avenue, NW, Suite 600
Grand Rapids, Michigan 49503
616-742-3500

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11SEP01 E658911-1 C63975
P01/7700 0.00-0121891.6

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Cardiff Road
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NP9 1RH

1. Your reference — 01.0098-Sen/P040/GB/AJW

2. Patent application number *(The Patent Office will fill in this part)* — 0121891.6 — 11 SEP 2001

3. Full name, address and postcode of the or of each applicant *(underline all surnames)* — **Sendo International Limited**
1601-3 Kinwick Center
32 Hollywood Road, Central, Hong Kong

Patents ADP number *(if you know it)* 820 313 5001

If the applicant is a corporate body, give the country/state of its incorporation — **Hong Kong**

4. Title of the invention — INTEGRATED CIRCUIT PACKAGE AND PRINTED CIRCUIT BOARD ARRANGEMENT

5. Name of your agent *(if you have one)* — ~~Antony Wray~~

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)* — ~~Inetip~~
~~121 Blackberry Lane~~
~~Four Marks, Alton~~
~~Hampshire GU34 5DJ~~
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51/77
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Patents ADP number *(if you know it)* 7922958002

	Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*
6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number			

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7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application		

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b) there is an inventor who is not named as an applicant, or
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See note (d)) — **Yes**

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Description	14
Claim(s)	3
Abstract	1
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Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	
Request for preliminary examination and search *(Patents Form 9/77)*	
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature A J Wray Date 11 September 2001

12. Name and daytime telephone number of person to contact in the United Kingdom **Antony Wray** **01256 816233**

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Statement of inventorship and of right to grant of a patent

1. Your reference: 01.0098-Sen/P040/GB/AJW

2. Patent application number *(If you know it)*:

3. Full name of the or of each applicant: **Sendo International Limited**
1601-3 Kinwick Center
32 Hollywood Road, Central, Hong Kong

4. Title of the invention: **INTEGRATED CIRCUIT PACKAGE AND PRINTED CIRCUIT BOARD ARRANGEMENT**

5. State how the applicant *(s)* derived the right from the inventor *(s)* to be granted a patent: **The applicant derives the right to be granted a patent by virtue of the inventor's employment agreement with Sendo Ltd. in Small Heath Business Park, Birmingham, England - a sister company of the applicant – in conjunction with a written agreement transferring all IP rights from Sendo Ltd. to the applicant. Sendo International Ltd.**

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7. I/We believe that the person *(s)* named over the page *(and on any extra copies of this form)* is/are the inventor *(s)* of the invention which the above patent application relates to.

Signature: A J Wray

Date: 11 September 2001

8. Name and daytime telephone number of person to contact in the United Kingdom: **Antony Wray** **01256 816233**

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

Olivier BOIREAU,

19 Oxford Drive
Birmingham
West Midlands
B27 6SH

Patents ADP number *(if you know it)*: 8228132001

Patents ADP number *(if you know it)*:

Patents ADP number *(if you know it)*:

Reminder

Have you signed the form?

INTEGRATED CIRCUIT PACKAGE AND PRINTED CIRCUIT BOARD ARRANGEMENT

Field of the Invention

The present invention relates to an integrated circuit package and circuit board arrangement. The invention is applicable to, but not limited to, a contact layout arrangement for integrated circuit packaging.

Background of the Invention

Most, if not all, current electrical and electronic equipment uses printed circuit board (PCB) technology to operably couple electronic components together. A typical printed circuit board includes a large number of metalised tracks to facilitate the operable coupling of components.

Such components typically have a plurality of contact points, such as input/output ports, power supply points, ground points, clock signal input/output ports, etc., to interface to other components. In recent times, the complexity of such electronic components and circuits has increased dramatically, to the point now where many electronic components and functions are performed in single or multiple integrated circuit packages.

An integrated circuit (IC) is a complete circuit that is manufactured as a single package. The IC may consist of several separate component parts attached by a ceramic substrate and interconnected by wire bonds or a suitable metalisation pattern. The complexity of circuits being produced on a single chip has been increasing rapidly, where very large scale integration (VLSI) and extra large-scale integration (ELSI) having hundreds of thousands of logic gates on a single chip are becoming commonplace.

Consequently, printed circuit boards have become more complex to design, to facilitate the increase in the number of tracks to link to the various component parts of the IC. As such, in the main, printed circuit boards have evolved to multi-layer arrangements, where each layer contains many tracks. The individual layers are operably connected at strategically designed points using vias, which are metallic connections that link two or more layers in a multi-layer substrate.

In the field of this invention it is known that integrated circuit (IC) packaging has evolved to the situation where each IC package requires a large number of different types of contacts, for example ground contacts, power supply contacts, oscillator/clock contacts, data and other high speed contacts etc.

The inventor of the present invention has identified problems encountered when attempting to route tracks to/from the contacts of IC packaging. These problems are

often caused by the particular layout of the contacts of the IC package.

A first problem encountered relates to the power supply contacts of the IC package. As known in the art, power supply contacts require large de-coupling capacitors connected thereto. If a long track is provided between the capacitor and its corresponding power supply contact, the track acts as a resistor. The combination of the capacitance with the induced resistance effectively creates a filtering effect on the power supply signal input to the power supply contact on the IC package. The longer a track to the contact point, the greater is the resistance induced by the track. In this manner, by having a resistance between the capacitor and the power supply contact, the ability for current to flow between the resistor and the power supply contact is reduced. Hence, it is important to provide the shortest amount of track between the capacitor and the power supply contact.

Furthermore, because of the potentially high amount of current that can flow through power supply contacts and tracks, the tracks need to be relatively wide. Therefore, it is also preferable to keep the tracks as short as possible in order to reduce costs and reduce the amount of area on the PCB taken up by such power supply tracks.

A second problem encountered relates to ground connections of IC packages. The problem recognised by the inventor of the present invention relates to the

connecting of ground points, contacts and/or layers of an IC package using the aforementioned vias (sometimes termed through-holes), which pass through several layers of a PCB. For electronic devices such as mobile phones, the ground layer is often extended to substantially the entire length and width of the PCB, and designed to act as a shield between radio frequency (RF) circuitry and baseband circuitry. Because of this, baseband circuitry is often arranged to be on the opposite side of the ground-plane (or layer) to the RF circuits/components. Thus, such vias often provide obstructions when trying to route tracks around the PCB.

A third problem encountered arises from the need to connect timing or frequency contacts to oscillator or clock generation circuits, which are used by the IC to provide clock signals etc. These contacts are required to be connected to oscillators, such as quartz, and decoupling capacitors. If tracks used to connect to such components are again too long, parasitic capacitance and induced resistance become significant enough to affect the oscillating signal frequency, and thereby the resulting clock signal(s).

Thus, in order for clock signals to be as accurate as possible, the required components are preferably located as close to the integrated circuit package contacts as possible. Furthermore, clock signals on devices such as mobile phones are prone to interference caused by RF signals. Although the ground layer is often provided between baseband circuitry and RF circuitry, vias and

other inter-layer connections can cause apertures in the ground layer, which facilitate the propagation of RF interference.

A need therefore exists for an improved integrated circuit and printed circuit board arrangement, and, in particular, an improved contact layout configuration for an integrated circuit, wherein the abovementioned disadvantages may be alleviated.

Statement of Invention

In accordance with a first aspect of the present invention there is provided a printed circuit board as claimed in claim 1.

In accordance with a second aspect of the present invention, there is provided an integrated circuit package device, as claimed in claim 2.

In accordance with a third aspect of the present invention, there is provided an electrical or electronic device, as claimed in claim 6.

Further aspects of the invention are as claimed in the dependent claims.

In summary, the present invention proposes inter-alia, to arrange the positioning of an IC package's interface

ports/contact points to facilitate an easier, more accurate and more reliable printed circuit board layout.

Brief Description of the Drawings

Exemplary embodiments of the present invention will now be described, with reference to the accompanying drawings that illustrate preferred contact layouts for integrated circuit packages etc., in which:

FIG. 1 shows an IC package contact layout illustrating a positioning of power supply contacts and clock generation contacts, in accordance with the preferred embodiment of the present invention;

FIG. 2 shows an IC package contact layout illustrating positioning of ground contacts, in accordance with the preferred embodiment of the present invention; and

FIG. 3 shows an IC package contact layout illustrating positioning of contacts for data signals and other high speed signals, in accordance with the preferred embodiment of the present invention.

Description of Preferred Embodiments

Referring first to FIG. 1, an IC package contact layout 100, illustrating a preferred positioning of power supply contacts 130 and clock generation contacts 140, is shown.

The IC package layout of the preferred embodiment of the present invention includes an inner portion of contacts 120 and an outer portion of contacts 110.

The power supply contacts 130 are shown on the extremities of the outer portion of the IC package, illustrated as solid black circles. By selecting the extremities of the outer portion of an IC package as power supply contacts, shorter track paths from the power supply of the electronic device to the power supply contact point(s) of the IC package are achieved.

In addition, if required, clock generation contacts 140 are shown on the extremities of the outer portion of the IC package, illustrated as hashed circles. Similarly, this enables shorter track paths from the clock generation component(s) of the electronic device to the clock/timing contact point(s) of the IC package.

This topography allows the power supply contact(s) to be located as close as possible to its/their associated de-coupling capacitor(s), thereby minimising the track resistance introduced to the circuit. Beneficially, the area on the PCB taken up by the tracks to the power supply contact(s) is also minimised.

Furthermore, this topography allows the required clock generation components to be as close to the relevant clock/timing contact point(s) as possible. Hence, undesired parasitic capacitance and resistance due to the length of track(s) between the clock or frequency

generator components and the clock/timing contact point(s) are minimised to avoid affecting the timing signal(s). In addition, it enables the required clock signal tracks to be designed on the uppermost layer of the printed circuit board, thereby minimising any effect of interference from say RF circuits and components.

Referring now to FIG. 2, an IC package contact layout 200 illustrates a positioning of ground contacts in accordance with the preferred embodiment of the present invention.

Again, the IC package layout of the preferred embodiment of the present invention includes an inner portion of contacts 120 and an outer portion of contacts 110. The preferred positioning of the ground contacts are illustrated as solid black circles 220 on the inner portion of the IC package layout 200.

Hence, the preferred embodiment of the present invention provides the ground contacts of the integrated circuit package substantially towards the centre of the integrated circuit package. In this manner, the need for other contacts of the integrated circuit package to have to be routed around the ground contacts and their related vias is minimised. This topography is of significant benefit in the circuit layout design of baseband circuitry, which, with the above ground contacts, can now be more readily positioned distal from the RF circuitry.

components with a plurality of contact points, such as Programmable Gate Logic Arrays (PGLAs), Application Specific ICs (ASICs), etc. As such, it is envisaged that any electrical or electronic device comprising an integrated circuit package device would benefit from the inventive concepts described herein.

It will be understood that the various contact layout embodiments described above provide at least some of the following advantages:

(i) In arranging the power supply contacts in the extremity of the outer portion of contacts, the required de-coupling capacitors can be located as close to the power supply contacts as possible, thereby keeping the track length to a minimum.

(ii) By providing the ground contacts toward the centre of the IC package, avoids the need for the other contacts to be routed around the ground contacts and their related vias.

(iii) Provision of the timing and/or frequency contacts on the extremity of the outer portion, together with the power supply contacts, allows the required clock generation components etc. to be positioned as close to the respective contacts as possible, whilst enabling all required tracking to be arranged on the uppermost layer(s).

(iv) Provision of the data and/or high speed signal contacts on the internal side of the outer portion, allows easier access to these ports, particularly when in conjunction with implementing the arrangements in (i)-(iii).

Whilst the specific and preferred implementations of the embodiments of the present invention are described above, it is clear that one skilled in the art could readily apply variations and modifications of such inventive concepts.

Thus, an improved integrated circuit and printed circuit board arrangement has been described wherein the aforementioned disadvantages associated with prior art arrangements have been substantially alleviated.

Claims

1. An integrated circuit package device having a plurality of contact points, wherein the plurality of contact points of said at least one integrated circuit package device circuit board include an inner portion of contact points and an outer portion of said contact points, the integrated circuit package device comprising at least one of the following:

(i) one or more power supply contacts configured substantially in said outer portion of said integrated circuit package device;

(ii) one or more timing or frequency contacts substantially in said outer portion of said integrated circuit package device;

(iii) one or more ground contacts configured substantially in said inner portion of said integrated circuit package device; and

(iv) one or more data or high speed signal contacts configured substantially in said inner portion of said integrated circuit package device.

2. A printed circuit board having a plurality of tracks for operably coupling electrical signals to a plurality of contact points of at least one integrated circuit package device, wherein the plurality of contact points of said at least one integrated circuit package device circuit board include an inner portion of contact points and an outer portion of contact points, the printed circuit board comprising at least one of the following:

(i) one or more power supply contacts configured substantially in said outer portion of said integrated circuit package device;

(ii) one or more timing or frequency contacts substantially in said outer portion of said integrated circuit package device

(iii) one or more ground contacts configured substantially in said inner portion of said integrated circuit package device; and

(iv) one or more data or high speed signal contacts configured substantially in said inner portion of said integrated circuit package device.

3. The integrated circuit package device according to Claim 1 or the printed circuit board according to Claim 2, wherein the ground contacts are further provided along a bisectional axis, through said outer portion of contacts to facilitate a ground path from outside an area of the integrated circuit to said inner portion.

4. The integrated circuit package device according to Claim 1 or Claim 3 or the printed circuit board according to Claim 2 or Claim 3, wherein said inner portion is formed substantially of ground contact points to effect a ground plane.

5. The integrated circuit package device according to Claim 1, or the printed circuit board according to Claim 2, wherein, for one or more of said signals associated with (i) to (iv), all of said respective contacts of said

integrated circuit are configured in the respective manner described in one or more of (i) to (iv).

6. An electrical or electronic device comprising the integrated circuit package device according to claim 2.

7. A printed circuit board substantially as hereinbefore described with reference to, and/or as illustrated by, FIG. 1, FIG. 2 or FIG.3 of the accompanying drawings.

8. An integrated circuit package device substantially as hereinbefore described with reference to, and/or as illustrated by, FIG. 1, FIG. 2 or FIG.3 of the accompanying drawings.

INTEGRATED CIRCUIT PACKAGE AND PRINTED CIRCUIT BOARD ARRANGEMENT

Abstract

An integrated circuit package device (100, 200, 300) has a plurality of contact points including an inner portion of contact points (120) and an outer portion of contact points (110). The integrated circuit package device includes at least one of the following: (i) one or more power supply contacts (130) configured substantially in said outer portion; (ii) one or more ground contacts (220, 230) configured substantially in said inner portion; (iii) one or more timing or frequency contacts (140) substantially in said outer portion; (iv) one or more data or high speed signal contacts (310) configured substantially in said outer portion of said integrated circuit package device.

This provides the advantage that the required capacitors can be located as close to the power supply contacts as possible, and the tracking to these contacts can be kept to a minimum. Furthermore by providing the ground contacts toward the inner portion of the integrated circuit package device, the need for the other contacts to be routed around the ground contacts and any related vias is avoided.

(FIG. 1 to accompany abstract)

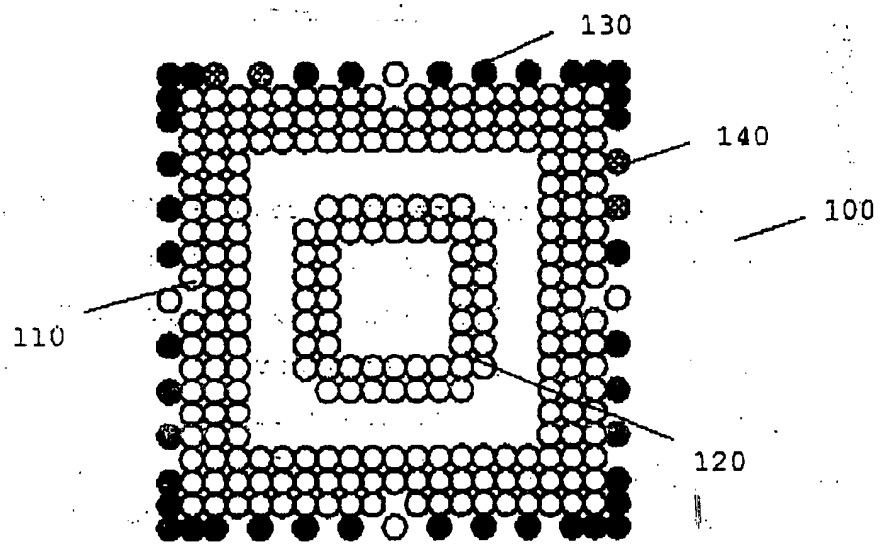

FIG. 1

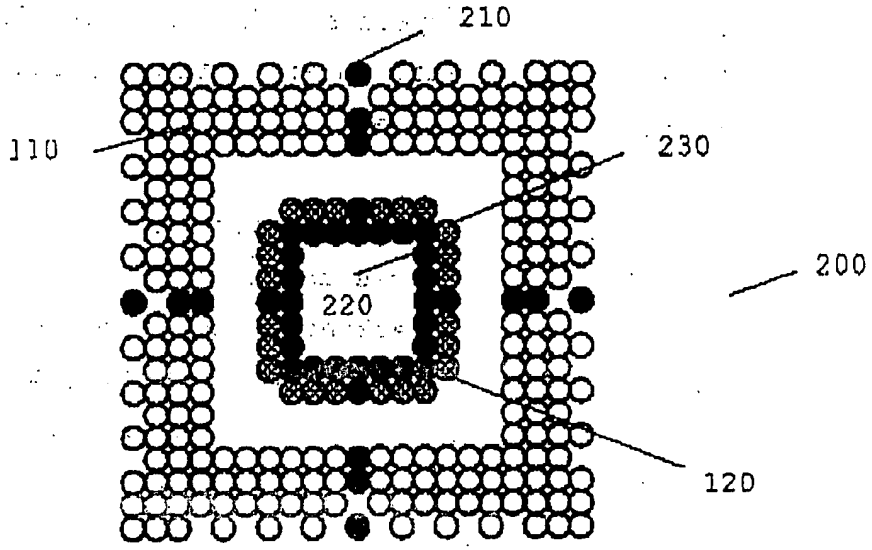

FIG. 2

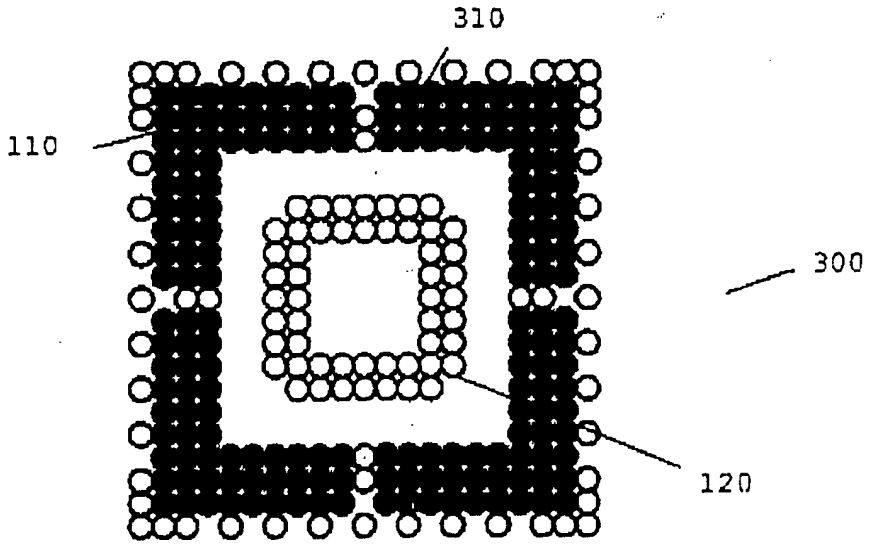

FIG. 3